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Performance Analysis of an NoC for Multiprocessor SoC

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Abstract

In this work focus on 'Network on chip' and "Multiprocessor system on chip" applications its a guaranteed supporting for network process to reducing the circuit area, lower power consumption, low cost, and increases the performance. Network employs multi-stage network approaches on packet switching and pipelined circuit switching. Based on packet switching need more buffers, area should be high. To overcome the occupy more area by using pipelined circuit switching reducing some buffers in a multiple networks, The proposed network employs CHIPPER (Cheap-Interconnect Partially Permuting Router) technique for using "bufferless deflection router" method. This bufferless deflection routers to eliminate route buffers and cross buffers. So Removing buffers yields more energy in network on chip.

Keywords : Buffer less deflection routers, Chipper tecniques, FPGA, Multiprocessor system on chip, Multistage interconnets, Network onchip.

Introduction

Multiprocessor system on chip are the only way to achieve high signal processing used to interconnected with on-chip network is currently emergimg for applications of parallel processing, significant, and so on. While Limiting The Power Consumption through the use of specialised processing elements and architecture. Network on chip technology applies networking theory and methods to on-chip communication and brings notable improvements over conventional bus and crossbar interconnections. Network on chip improves the scalability of SoC.

An MPSoC is a system on-chip in VLSI system that incorporates most or all the components necessary for an application that uses multiple programmable Processors as system components. MPSoCs are widely used in networking, communications, signal processing. NoC is constructed from multiple point to point data links connected by switches (routers although packet switching is sometimes claimed as necessity for a NoC, there are types of NoC proposals occurred circuit switching, multiprocessor system on chip (MPSoC).

In this work we proposed bufferless router **CHIPPER** (Cheap Interconnect Partially Permuting Router) rearranging the crossbar switch by using buffers hence to be reduced. Further reducing the critical path length and power/area cost.

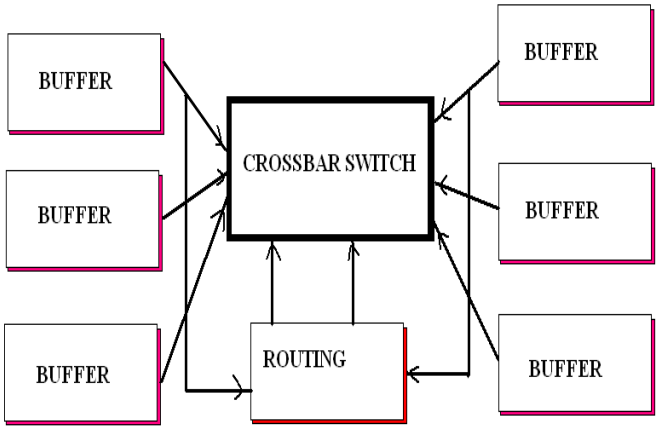

Fig.1 A single crossbar switch or point to point networks scheme.

Related Works

A system-level design environment for the generation of bus-based system-on-chip architectures[1]. Our approach supports a two-stage design flow using automated model refinement toward custom communication networks. Starting from an abstract specification of the desired communication channels, our environment automatically generates tailored network models at

various levels of abstraction. At its core, an automatic layer-based refinement approach is utilized. We have applied our approach to a set of industrial-strength examples with a wide range of target architectures.

In that chip multiprocessors (CMPs) that accommodate multiple processor cores on the same chip have become a reality.As the communication complexity of such multicore systemic rapidly increasing, designing an interconnect architecture with predictable behavior is essential for proper system operation. In CMPs, general-purpose processor cores are used to run software tasks of different applications and the communication between the cores cannot be pre-characterized. Designing an efficient network-on-chip (NoC)-based interconnect with predictable performance is thus a challenging task. In this paper, we address the important design issue of synthesizing the most power efficient NoC interconnect for CMPs, providing guaranteed optimum throughput and predictable performance for any application to be executed on the CMP. In our synthesis approach, we use accurate delay and power models for the network components (switches and links) that are obtained from layouts of the components using industry standard tools. The synthesis approach utilizes the floor plan knowledge of the NoC to detect timing violations on the NoC links early in the design cycle. This leads to a faster design cycle and quicker design convergence across the high-level synthesis approach and the physical implementation of the design. We validate the design flow predictability of our proposed approach by performing a layout of the NoC synthesized for a 25-core CMP. Here many-core design paradigm requires flexible and modular hardware and software components to provide the required scalability to next generation on-chip multiprocessor architectures.

A multidisciplinary approach is necessary to consider all the interactions between the different components of the design [7]. In this paper, a complete design methodology that tackles at once the aspects of system level modeling, hardware architecture, and programming model has been successfully used for the implementation of a multiprocessor network-on-chip (NoC)-based system, the NoC Ray graphic accelerator. The design, based on 16 processors, after prototyping with field-programmable gate array (FPGA), has been laid out in 90-nm technology. Post-layout results show very low power, area, as well as 500 MHz of clock frequency. Results show that arrays of small and simple processors outperform a single high-end general purpose processor.

We present network-on-chip (NoC) design[3]and contrast it to traditional network design, highlighting similarities and differences between the two. As an initial case study, we examine network congestion in buffer less NoCs. We show that congestion manifests itself differently in a NoC than in traditional networks. Network congestion reduces system throughput in congested workloads for smaller NoCs (16 and 64 nodes), and limits the scalability of larger buffer less NoCs (256 to 4096 nodes) even when traffic has locality (e.g., when an application's required data is mapped nearby to its core in the network).We propose a new source throttling based congestion control mechanism with application-level awareness that reduces network congestion to improve system performance[3].Our mechanism improves system performance by up to (28% (15% on average in congested workloads) in smaller NoCs, achieves linear throughput scaling in NoCs up to 4096 cores attaining similar performance scalability to a NoC with large buffers), and reduces power consumption by up to 20%. Thus, we show an effective application of a network-level concept, congestion control, to a class of networks – buffer less on-chip networks – that has not been studied before by the networking community.

A Designing a power-efficient interconnection architecture for Multiprocessor system on chips (MPSoC) satisfying the application performance constraints is a nontrivial task. In order to meet the tight time-to-market constraints and to effectively handle the design complexity, it is essential to provide a computer-aided design tool support for automating this task. In this paper, we address the issue of "application-specific design of optimal crossbar architecture" satisfying the performance requirements of the application and optimal binding of the cores onto the crossbar resources.

We present a simulation-based design approach that is based on the analysis of the actual traffic trace of the application, considering local variations in traffic rates, temporal overlap among traffic streams, and criticality of traffic streams. Our approach is physical design aware, where the wiring complexity of the crossbar architecture is also considered during the design process. This leads to detecting timing violations on the wires early in the design cycle and to having accurate estimates of the power consumption on the wires. We apply our methodology onto several MPSoC designs, and the synthesized crossbar platforms are validated for performance by cycle-accurate System simulation of the designs. The crossbar matrix power consumption values are based on the synthesis of the register transfer level models of the designs, obtained using industry standard tools.

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The experimental case studies show large reduction in communication architecture power consumption (45.3% on average) and total wire length (38% on average) for the MPSoC designs when compared with traditional design approaches. The synthesized crossbar designs also lead to large reduction in transaction latencies (up to 7×) when compared with the existing design approaches.

Proposed Method

In chipper techniques constrained as two functional regions as following as

1. ejector/injector
2. Permuter

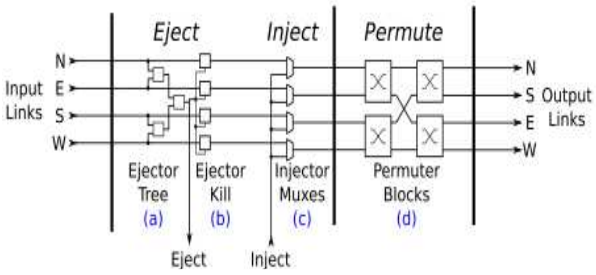

Fig.2 Buffer are re-placed by using permuter network without using control bus and data bus

Injection and Ejection We must now consider injection and ejection in this arbiter. So far, we have assumed four input ports and four output ports, without regard to the flit, local, router port. We could extend the permutation network to a fifth input and output. The ejection port can only accept a flit destined for the local node, and injection can only occur when there is a free slot (either because of an empty input link or because of an ejection). We instead handle ejection and injection as a separate stage prior to the arbitration network. The ejector and the injector, in the data path. This allows the stages to insert and remove flits before the set of four input flits reaches the arbiter.

A permutation network replaces the traditional arbitration logic and crossbar. Requires a wide age field in the packet header, and large comparators in the arbiter. We wish to avoid this expense, even if it may sacrifice a little performance. We start with the explicit goal of preserving livelock freedom, while stripping away anything unnecessary for that property. will eventually be delivered.

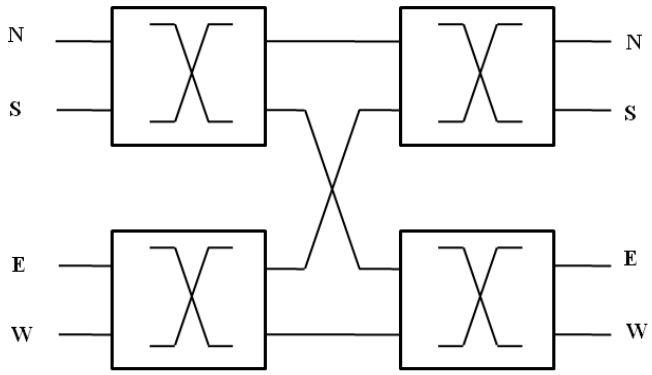

Fig.3 Interconnection of Permuter Networks

We observe that it is sufficient to pick a single packet, and prioritize that packet globally above all other packets for long enough that its delivery is ensured. If every packet in the system eventually receives this special status, then every packet.

Results and Performance Comparison

As Performance of an **CHIPPER** Techniques are Given Below, in that 4 inputs and 4 outputs LUT's by analyzing the interconnect designs.

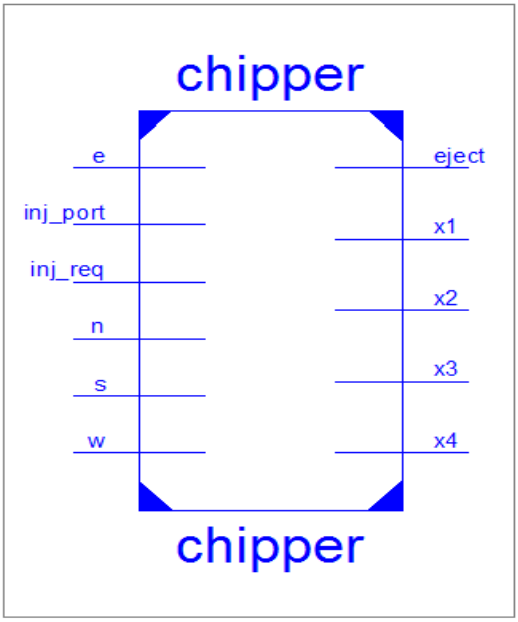

Fig.4 Input/Outputs LUT'S Port

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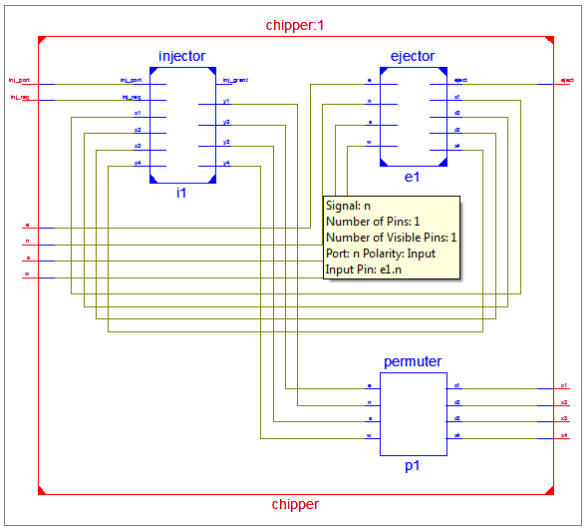

Fig.5 combinational ports

The above figure shows the injector/ejector and permuter, inputs and output LUT's

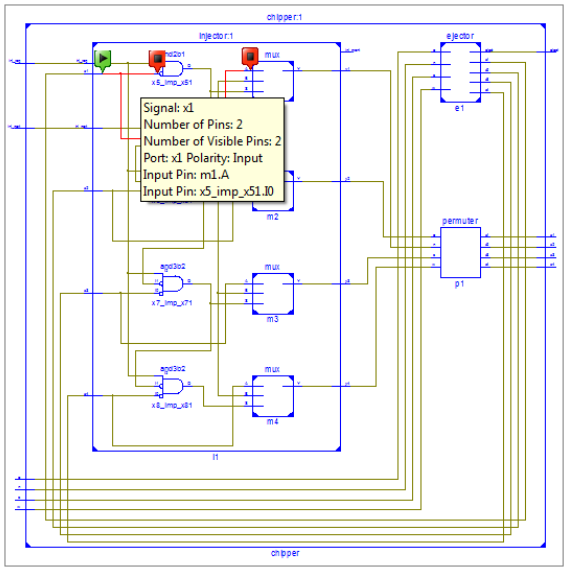

Fig.6 interconnections between the each port

The above figure shows permuter outputs LUT's interconnections.

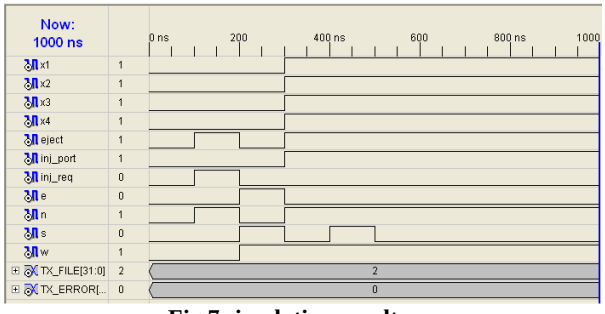

Fig.7 simulation results

The above fig shows permutated results of an area minimization.

Table I

EXISTING: Analysis and Performance of Circuit Switching and Packet Switching method

LOGIC UTILIZATION	Used	Available	Utilization
Number of 4 input LUTS	4	9,312	1%
LOGIC DISTRIBUTION			
Number of Occupied Slices	30	4,656	1%
Number of Slices containing only related logic	30	30	100%
Number of Slices containing unrelated logic	0	30	0%
Total Number of 4 input LUTs	55	9,312	1%
Number of bonded IOBs	22	232	9%

Table II

PROPOSED: Analysis and Performance of **CHIPPER** Method

LOGIC UTILIZATION	Used	Available	Utilization
Number of 4 input LUTS	7	9,312	1%
Logic distribution			
Number of Occupied slices	4	4,656	0%
Number of slices containing only related logic	4	4	100%
Number of slices containing unrelated logic	0	4	0%
Total number of 4 input LUTS	7	9,312	1%
Number of bonded IOBS	11	232	4%

Conclusion

In that we have presented as design for buffer less deflection router (**CHIPPER**) networks by used cheap-interconnect partially permuting router networks, to reduces the area 75% compared then existing method. The hardware complexity reduced

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as well as Significant energy savings (78.5% even in dense networks and perfect caches) also reduced. It's our hope that this will inspire more ideas and further work on cheap interconnect design.

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